IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	: Jeffrey S. Brown	Group Art Unit: 2825
Appln. No.:	09/878,499	Examiner: A. Thompson
Filed	: June 11, 2001	
For	: HARD MACRO HAVING IMPROVED PORT ROUTING	
Docket No.:	L13.12-0154/00-674	

DECLARATION OF PRIOR INVENTION IN THE UNITED STATES (37 C.F.R. § 1.131)

Commissioner for Patents
Washington, D.C. 20231

I HEREBY CERTIFY THAT THIS PAPER IS BEING SENT BY U.S. MAIL, FIRST CLASS, TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231, THIS

20TH DAY OF JANUARY, 2004.

PATENT ATTORNEY

INVENTORSHIP IDENTIFICATION

As a person signing below, I hereby declare that:

1. I am a co-inventor of the subject matter claimed in the above-identified patent application.
2. My residence, post office address and citizenship are as stated below next to my name.
3. I am an employee of LSI Logic Corporation.
4. Exhibit A is a redacted copy of our LSI Logic Invention Disclosure form, which we submitted to the LSI Logic legal department prior to June 4, 2001.
5. Exhibit B is a redacted print out of an LSI Logic Corporation database log as of January 4, 2004. This database log includes dates of events relating to the Invention Disclosure shown in Exhibit A.

CONCEPTION

6. I jointly conceived in the United States the subject matter claimed in the above-identified patent application prior to June 4, 2001, which is the alleged priority date for U.S. Publication No. 2002/0184601 A1 (Fitzhenry et al.).
7. Exhibit A contains a detailed description of various embodiments of the invention. See Exh. A, pgs. 3-4.
8. Exhibit B shows that on May 11, 2001, a first draft of a patent application disclosing and claiming the invention described in the invention disclosure shown in Exhibit A was received by LSI Logic. See Exhibit B, page 1.
9. Both Exhibits A and B show that as of May 11, 2001, a date earlier than the alleged effective date of Fitzhenry et al., the conception of the invention was in our minds as a definite and permanent idea.

DILIGENCE

10. As an inventor, I was diligent in constructively reducing the invention to practice from a date prior to the effective date of Fitzhenry et al. until the filing of the application on June 11, 2001.
11. The redacted version of Exhibit B shows log entries from May 11, 2001 through the filing of the application on June 11, 2001. According to Exhibit B, on May 11, 2001, a draft of the application disclosing and claiming the invention described in the invention disclosure of Exhibit A was received for review. On May 14, 2001, the attorney received comments on the draft application from an inventor. Between May 14, 2001 and June 8, 2001, additional comments on the application were exchanged and revisions to the application were made. On June 8, 2001, a final draft of the application

was received by LSI Logic. Between June 8, 2001 and June 11, 2001, the necessary signatures of the below-named inventors were obtained. On June 11, 2001, the application was filed with the United States Patent and Trademark Office.

DECLARATION

I declare that all statements made herein that are of my own knowledge are true and that all statements that are made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURES

Inventor: _____ (Signature) Date: 1/16/2004

Inventor: Jeffrey S. Brown

Residence: Fort Collins, Colorado Citizenship: U.S.A.

P.O. Address: 3624 Goodell Lane, Fort Collins, Colorado 80526

Inventor: Craig R. Chafin Date: 1/16/04
(Signature)

Inventor: Craig R. Chafin

Residence: Colorado Springs, Colorado Citizenship: U.S.A.

P.O. Address: 627 Paradise Lane, Colorado Springs, Colorado 80904

Respectfully submitted,

WESTMAN, CHAMPLIN & KELLY, P.A.

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BDK/djb

BEST AVAILABLE

LSI LOGIC – INVENTION DISCLOSURE FORM

Disclosure No. CO 00-674

1. INVENTOR(S)

A. NAME: Jeff Brown M/S - AQ220
HOME ADDRESS: 3624 Goodell Lane, Fort Collins, CO 80526
[redacted]
HOME PHONE: [redacted]
CITIZENSHIP: US

B. NAME: Craig Chafin M/S - AQ220
HOME ADDRESS: 1601 W Swallow Rd #6H, Fort Collins, CO 80526
EXT. [redacted]
HOME PHONE: [redacted]
CITIZENSHIP: US

C. DIVISION, DEPARTMENT, SUBSIDIARY: Memory and Mixed Signal - CO Dept.107681

2. TITLE OF THE INVENTION (MUST BE FILLED OUT): Enhanced Hard Macro Port Routing Methodology

3. CONCEPTION OF THE INVENTION

A. DATE OF FIRST DRAWING: [redacted]
WHERE CAN FIRST DRAWING BE FOUND? This document

B. DATE OF FIRST WRITTEN DESCRIPTION: [redacted]
WHERE IS DESCRIPTION FOUND? This document

C. [redacted]

4. CONSTRUCTION OF DEVICE

A.	DATE COMPLETED	N/A
B.	WAS PROTOTYPE MADE?	N/A
C.	BY WHOM MADE?	N/A
D.	WHERE CAN PROTOTYPE BE FOUND?	N/A

5. TEST OF DEVICE

RECEIVED
LSI LOGIC CORP
INTELLECTUAL PROPERTY DEPT

A.	DATE	N/A
B.	WITNESS	[redacted] N/A
C.	RESULT	N/A

6. SALE

A.	WAS INVENTION SOLD?	YES	NO XXX
B.	DATE OF FIRST SALE	N/A	

7. USE

A.	IS THE INVENTION PRESENTLY BEING USED?	YES	NO XXX
B.	ARE THERE SPECIFIC PLANS FOR ITS USE IN THE NEAR FUTURE?	YES XXX	NO

EXHIBIT tabbies A

INVENTORS:

Jeff R — DATE [redacted]
Craig Chafin — DATE [redacted]

WITNESS. READ AND UNDERSTOOD BY:

(PRINT) Mark Jetton (SIGN) Mark Jetton DATE [redacted]
(PRINT) Ellen Pihlstrom (SIGN) Ellen Pihlstrom DATE [redacted]

(EACH PAGE UPON WHICH INFORMATION IS ENTERED SHOULD BE SIGNED AND WITNESSED)

LSI LOGIC

- INVENTION DIS[illegible]SURE FORM

Disclosure No.

[redacted]

	WAS INVENTION		
	A. [redacted]	[redacted]	[redacted]
	B. [redacted]	[redacted]	[redacted]
	C. [redacted]	[redacted]	[redacted]
	D. [redacted]	N/A CONTRACT NUMBER	
10.	WAS INVENTION		
	A. [redacted]	[redacted]	[redacted]
	B. [redacted]	[redacted]	[redacted]
	C. [redacted]	[redacted]	[redacted]
	D. [redacted]	N/A CUSTOMER	

THIS DESCRIPTION OF THE INVENTION SHOULD BE WRITTEN IN THE INVENTOR'S OWN WORDS AND GENERALLY SHOULD FOLLOW THE OUTLINE GIVEN BELOW. SKETCHES, PRINTS, PHOTOS AND OTHER ILLUSTRATIONS, AS WELL AS REPORTS OF ANY NATURE IN WHICH THE INVENTION IS REFERRED TO, IF AVAILABLE, SHOULD FORM A PART OF THIS DISCLOSURE AND REFERENCE CAN BE MADE THERETO IN THE DESCRIPTION OF CONSTRUCTION AND OPERATION:

USE THE ATTACHED SHEETS TO ANSWER THE FOLLOWING QUESTIONS.
(Attach Engineering Reports or other documentation to this form.)

1.	GENERAL PURPOSE OF THE INVENTION. STATE IN GENERAL TERMS THE OBJECTS OF THE INVENTION.
2.	DESCRIBE OLD METHOD(S), IF ANY, OF PERFORMING THE FUNCTION OF THE INVENTION.
3.	INDICATE THE DISADVANTAGES OF THE OLD METHOD(S).
4.	DESCRIBE THE CONSTRUCTION OF YOUR INVENTION, SHOWING THE CHANGES, ADDITIONS AND IMPROVEMENTS OVER THE OLD METHOD.
5.	GIVE DETAILS OF THE OPERATION IF NOT ALREADY DESCRIBED UNDER 4.
6.	STATE THE ADVANTAGES OF YOUR INVENTION OVER WHAT HAS BEEN DONE BEFORE.
7.	INDICATE ANY ALTERNATE METHOD OF CONSTRUCTION.
8.	IF A JOINT INVENTION, INDICATE WHAT CONTRIBUTION WAS MADE BY EACH INVENTOR.
9.	FEATURES WHICH ARE BELIEVED TO BE NEW.
10.	STATE OPINION OF RELATIVE VALUE OF THE INVENTION.
11.	AFTER THE DISCLOSURE IS PREPARED, IT SHOULD BE SIGNED BY THE INVENTOR(S) AND THEN READ AND SIGNED BY TWO WITNESSES IN THE SPACE PROVIDED AT THE BOTTOM OF EACH SHEET.

INVENTORS:

[redacted] DATE [redacted]

[redacted] DATE [redacted]

WITNESS, READ AND UNDERSTOOD BY:

(PRINT) Mark Jetton (SIGN) Mark Jetton DATE [redacted]

(PRINT) Ellen Pihlstrom (SIGN) Ellen Pihlstrom DATE [redacted]

(EACH PAGE UPON WHICH INFORMATION IS ENTERED SHOULD BE SIGNED AND WITNESSED)

LSI LOGIC

LSI LOGIC - INVENTION DISCLOSURE FORM	Disclosure No.

1. General purpose - The purpose of the invention is to enhance the failure analysis capability of hard macros on an ASIC as well as eliminate any antenna rule violations after routing.

2. Old methods - Old methods would have the ports of a hard macro come out on any of several available routing layers. Usually this was a lower level metal layer that is buried and not easily accessible when the chip is completely built. Any failure analysis work to get at the inputs to the hard macro would be difficult. Also, when routing signals to the inputs of the hard macros, the routing tool might induce antenna rule violations where a large section of metal is hanging on the input gates without a drain area connected to it until a higher level metal is deposited. The routing tool would then need to have the functionality to go back into those routes and fix those problems.

3. Disadvantages of the old methods - Failure analysis work is difficult since the ports are hidden and the routing tool has to be smart enough to fix antenna rule violations after routing.

4. Construction of invention - Hard macro ports would still be routed into the cell at the usual lower level metal for port routing, but right inside the hard macro, the signal would be propagated up to the highest level metal used on the chip and then brought back down to the standard port metal layer inside the hard macro.

5. More details - The figure shows an input port to a hard macro on Metal2. This particular example assumes a 4LM chip, so the signal is pulled up to Metal4 and then brought back down to poly for the input transistor. This allows the hard macro ports to be easily accessible for failure analysis work. Whenever there's a problem with a hard macro, the first thing that needs to be looked at is the input/output signals at the ports. This also alleviates antenna rule violations as a result of chip level routing. The metal area hanging on the gate to the input device is minimized and isn't connected to anything else until there's a drain area from a cell driving the net also connected to the same net by the top level metal. Propagating the signal to the highest level of metal at the hard macro port guarantees that.

6. Advantages over what has been done before - Failure analysis is easier and the routing tool doesn't have to support fixing antenna rules for hard macros.

7. Method of alternative construction - Ports could be pulled up to the highest metal layer just for the sake of failure analysis work without having a short run of the highest level metal which is the part that gets rid of the antenna rule violations (ie. just a stack of vias to the top level of metal, but leaving the routing at the lower level). Diodes (drain areas) can also be added to the inputs to eliminate the antenna rule violations.

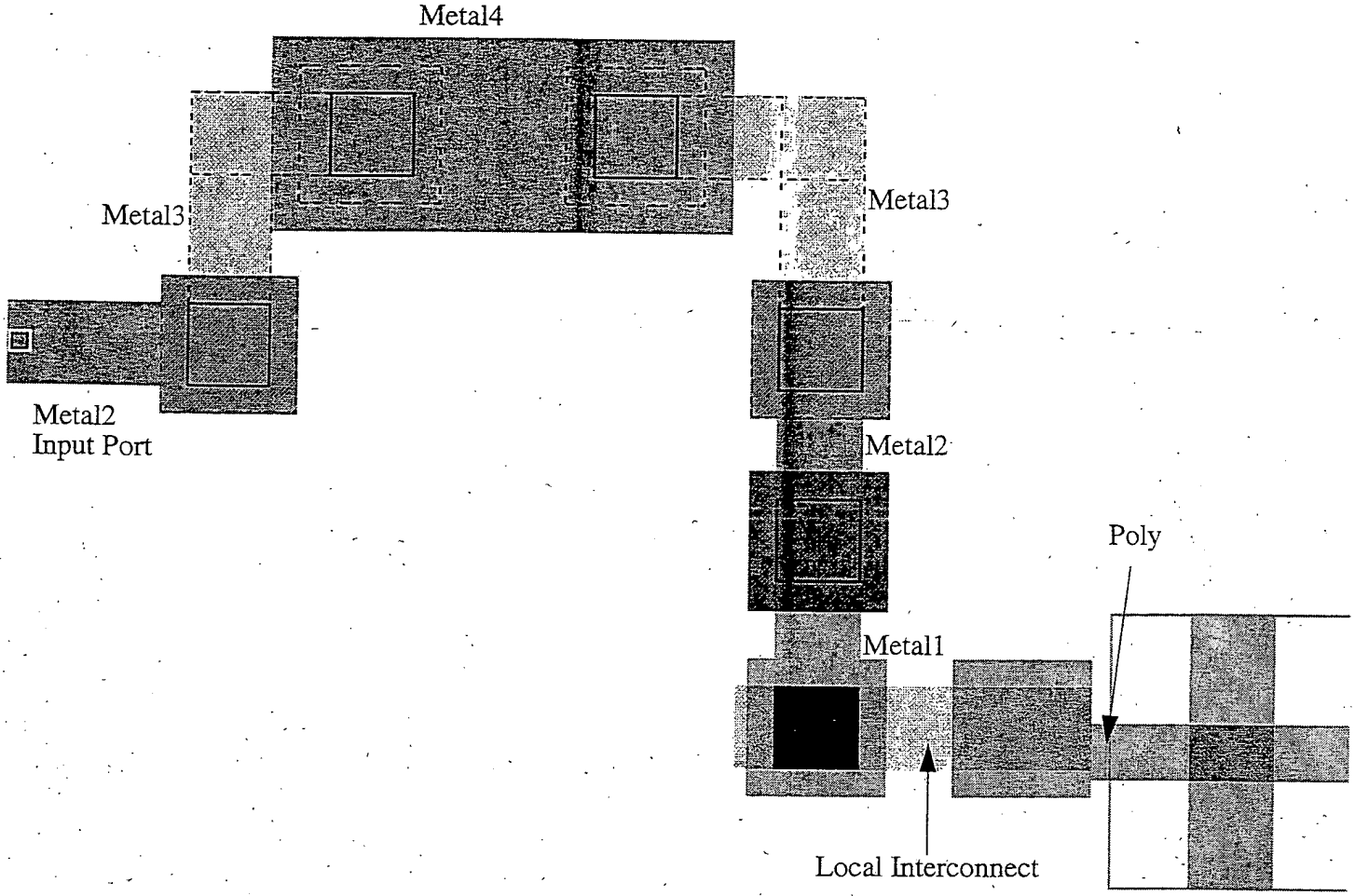
8. Joint invention - Yes.

[redacted]

INVENTORS:			LSI LOGIC [redacted]
[redacted]		DATE [redacted]	
[redacted]		DATE [redacted]	
WITNESS, READ AND UNDERSTOOD BY:			
(PRINT) Mark Jetton	(SIGN) Mark Jetton	DATE [redacted]	
(PRINT) Ellen Pihlstrom	(SIGN) Ellen Pihlstrom	DATE [redacted]	
~~(EACH PAGE UPON WHICH INFORMATION IS ENTERED SHOULD BE SIGNED AND WITNESSED)~~			PAGE 3

[redacted]

10. Opinion of value - This is highly valuable in a complex design flow where it is difficult to support antenna rule fixes through automation and also adds value in that the hard macro is inherently easy to access for failure analysis work. The only disadvantages are that some top level routing tracks will be occupied by the jumpers, but in most cases, the routing is already blocked over the hard macros.



INVENTORS:

[redacted] DATE [redacted]

[redacted] DATE [redacted]

WITNESS, READ AND UNDERSTOOD BY:

(PRINT) Mark Jetton (SIGN) [redacted] DATE [redacted]

(PRINT) Ellen Pihlstrom (SIGN) [redacted] DATE [redacted]

(EACH PAGE UPON WHICH INFORMATION IS ENTERED SHOULD BE SIGNED AND WITNESSED)

LSI LOGIC

1 Enhanced Hard Macro Port Routing Methodology

Inventor(s):

1 Jeff Brown

2 Craig Chafin

Type of Matter : Parent

Country of activity : United States

LSI Paralegal :

LSI Attorney :

Patent Liaison :

LSI VP/Manager :

Outside Counsel : Brush, David-WESTMAN, CHAMPLIN & KELLY- (612) 330-0484

Law Firm docket : L13.12-0154

Foreign Filing is NOT requested.

Ratings

Internal Use	*External Use*	*Novelty*	*Detectability*	*Life Cycle*	*Overall Rating*
2	2	2	2	2	4.04

Status of Matter : **Abandoned** **Technology :** Circuit

Serial Number : 09/878,499

13 Fri, May 11, 2001 Received 1st Draft
14 Mon, May 14, 2001 Commn. from Inventor - Received
15 Fri, Jun 08, 2001 Received Final Draft
16 Mon, Jun 11, 2001 Filed w/PTO with formals

EXHIBIT
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B

[redacted]

Keywords :

01 . Antenna: EDA/CAD - Signa
02 . I/O Circuit - Circuit (g
03 . Metallization Process - Metalliz

Billing	Type of transaction	Entry	Invoice	Firm
[redacted]				